AMENDMENTS TO THE SPECIFICATION

On page 1, please amend the paragraph beginning at line 4 as follows.

--The invention relates to an infrared detecting device.--

On page 6, please amend the paragraph beginning at line 8 as follows.

--The suppression circuit may comprise a resistor, a constant voltage supply circuit, a switch and a switch controlling circuit. The resistor is connected in series between the voltage amplification circuit and the detection circuit. The constant voltage supply circuit supplies a constant voltage between the resistor and the detection circuit through the switch. The switch is connected between ~~from~~ the constant voltage supply circuit and a pathway from ~~to~~ the resistor ~~and~~ to the detection circuit. The switch also opens or closes a pathway from the constant voltage supply circuit to the resistor and the detection circuit in response to OFF or ON signal from the switch controlling circuit respectively. The switch controlling circuit provides the ON signal to the switch from the start point. The switch controlling circuit also provides the OFF signal to the switch after the time period.--

On page 7, please amend the paragraph beginning at line 21 as follows.

--The suppression circuit may comprise a constant voltage supply circuit, a switch and a switch controlling circuit. The constant voltage supply circuit supplies a constant voltage to the detection circuit through the switch. The switch ~~is connected between from~~ exists at a junction connecting the constant voltage supply circuit, ~~and~~ the voltage amplification circuit ~~to~~, and the detection circuit. The switch also closes or opens a pathway (hereinafter referred to as a "first pathway") between the constant voltage supply circuit and the detection circuit in response to suppression or unsuppression signal from the switch controlling circuit respectively. The switch also opens or closes a pathway (hereinafter referred to as a "second pathway") between the voltage amplification circuit and the detection circuit in response to the suppression or the unsuppression signal respectively. The switch controlling circuit provides the suppression signal

to the switch from the start point. The switch also provides the unsuppression signal to the switch after the time period. Since the first and the second pathways are closed and opened during the time period, it becomes possible to prevent false operation due to variation when the drive current is changed over.--

On page 11, please amend the paragraph beginning at line 9 as follows.

--The device A comprises a drive power supply circuit 10 as a characteristic of the embodiment in addition to comprising a pyroelectric element 15, an I/V conversion circuit 16, a voltage amplification circuit 17, a detection circuit 18 and an output circuit 19~~ as well~~ in the same way as the prior art devices.--

On page 14, please amend the paragraph beginning at line 24 as follows.

--The variable current source 123 is constructed with NMOS transistors 123b, 123c and 123d and switch elements 123f and 123g~~ as well~~ in the same way as the source 122. The variable current source 124 is constructed with NMOS transistors 124b, 124c and 124d and switch elements 124f and 124g~~ as well~~ in the same way as the source 122.--

On page 15, please amend the paragraph beginning at line 20 as follows.

--The circuit 132 is constructed with PMOS transistors 132a and 132b~~ as well~~ in the same way as the circuit 131 and distributes the drive current based on the current from the source 122 to the voltage amplification circuit 17. The circuit 133 is constructed with PMOS transistors 133a and 133b~~ as well~~ in the same way as the circuit 131 and distributes the drive current based on the current from the source 123 to the detection circuit 18. The circuit 134 is constructed with PMOS transistors 134a and 134b~~ as well~~ in the same way as the circuit 131 and distributes the drive current based on the current from the source 124 to the output circuit 19.--

On page 20, please amend the paragraph beginning at line 5 as follows.

--The current generating circuit 22 comprises a common variable current source 222 as a characteristic of the embodiment in addition to comprising a reference current source 220 and a fixed current source 221 ~~as well~~ in the same way as the circuit 12 of the device A. The variable current source 222 further comprises a NMOS transistor 222e and a switch element (e.g., PMOS transistor) 222h as compared with the variable current source 122. Control terminals (gates) of the elements 222f-222h are connected to the terminals T211-T213 respectively. Gate of the NMOS transistor 215 is connected to the drain and the gate of the NMOS transistor 221a.--

On page 20, please amend the paragraph beginning at line 14 as follows.

--The distribution circuit 23 comprises a common current mirror circuit 232 as another characteristic of the embodiment in addition to comprising a current mirror circuit 231 ~~as well~~ in the same way as the circuit 13 of the device A. The current mirror circuit 232 further comprises a PMOS transistor 232c whose drain is connected to the detection circuit 28 and a PMOS transistor 232d whose drain is connected to the output circuit 29 as compared with the current mirror circuit 132.

On page 24, please amend the paragraph beginning at line 9 as follows.

--The device D is characterized by comprising a battery as a power source (not shown in FIG. 11), a mode changeover circuit 40D, a current changeover circuit 41 and a suppression circuit 44 in addition to comprising a pyroelectric element 45, an I/V conversion circuit 46, a voltage amplification circuit 47, a detection circuit 48 and an output circuit 49 ~~as well~~ in the same way as the device A.

On page 24, please amend the paragraph beginning at line 15 as follows.

--The mode changeover circuit 40D further comprises a holding circuit 400 while comprising a current generating circuit 42 and a distribution circuit 43 ~~as well~~ in the same way as the device A. The holding circuit 400 as shown in FIG. 12 holds state of output signal S49 of the

output circuit 49 for a prescribed time period T41. The state of S49 is held from a point in time (fall time of S48) when components-amplified voltage V47 by the circuit 47 becomes equal to a prescribed detection threshold voltage V481 or V482 of the detection circuit 48 or closer to a reference level ("offset" by bias voltage) Vb than the detection threshold voltage. Hereinafter the period T41 is also referred to as a "holding period" T41.--

On page 28, please amend the paragraph beginning at line 20 as follows.

--In this device E, an output of the voltage amplification circuit 57 is suppressed at 1x input voltage of the circuit 57 during the suppressing period. Therefore, by setting the suppressing period ~~as well~~ in the same way as the suppressing period T42 it becomes possible to prevent false operation due to variation when the drive current is stepped down.--

On page 29, please amend the paragraph beginning at line 20 as follows.

--In this device F, the pathway from the voltage amplification circuit 67 to the detection circuit 68 is opened during the suppressing period T62. Therefore, by setting the suppressing period T62 ~~as well~~ in the same way as the suppressing period T42 it becomes possible to prevent false operation due to variation when the drive current is stepped down.--

On page 30, please amend the paragraph beginning at line 22 as follows.

--In this device G, the first and the second pathways are closed and opened during the suppressing period. Therefore, by setting the suppressing period ~~as well~~ in the same way as the suppressing period T42 it becomes possible to prevent false operation due to variation when the drive current is stepped down.

On page 31, please amend the paragraph beginning at line 16 as follows.

--In this device H, the pathway is opened during the suppressing period. Therefore, by setting the suppressing period ~~as well~~ in the same way as the suppressing period T42 it becomes possible to prevent false operation due to variation when the drive current is stepped down.--

On page 32, please amend the paragraph beginning at line 8 as follows.

--The current generating circuit 92 comprises the above-mentioned common variable current source 922 in addition to a reference current source 920 and a fixed current source 921 with NMOS transistors 921a and 921b. The common variable current source 922 is constructed with NMOS transistors M1-Mn and switch elements (e.g., semiconductor switch element) SW2-SWn. The source 922 also provides variable current to a current mirror circuit 932 which is included in a distribution circuit 93 and constructed with PMOS transistors 932a-932d ~~as well~~ in the same way as FIG. 7.--